Advanced Computer Architecture

Credits: 4.00. **Prerequisite**: student must take course "VLSI CAD Systems and VLSI Architectures".

No exam in this course, only project (see below).

The goal of this course – to study the methodology for design and verification of pipelined processors from external specifications till the hardware implementation on chip with FPGA or ASIC technology.

Syllabus: Processor with pipeline architecture. Stages of pipelined processor – Fetch, Operands, Implement and Write. Transferring data between processor stages to create the parallel work of all stages. Transfers of instructions, addresses and operands. Skipping of pipeline stages. Hazards in pipelined processor. Dynamic instruction scheduling, branch prediction, instruction-level parallelism, multiple instruction fetch/issuing, speculative execution, etc. to improve computer processor performance. Structural hazard avoidance. Data hazard avoidance. Control hazard avoidance. Design methodology for pipelined processor. Design of the fast pipelined processor with complex addressing modes. High level design of each processor stages. Instruction description for each processor stage. Communication between each pair of stages. Behavior of each stage as a virtual Finite state machine. Design the functional test-bench for pipelined processor. Functional simulation of pipelined processor. Design of pipelined processor at the Register Transfer Level. Distribution of Data path components between processor stages. Design of pipelined processor with common Data path. Combining of Control units of all stages with common Data path. Top design of pipelined processor. Test-bench at the Register Transfer Level. Simulation of pipelined processor at the Register Transfer Level. Mapping of the processor netlist with ASIC or FPGA library tools. Place & Route for the processor netlist. Post Place & Route verification with ModelSim.

Project in the course. Each two student team will design their version of pipelined processor from external specification till implementation as ASIC (Cadence or Synopsis tools at the RTL level) or FPGA (Xilinx or Altera tools at the RTL level).

Bibliography:

Hennessy J., Patterson D., Computer Architecture: A Quantitative Approach, 5ed, Morgan Kaufmann Publishers, 2011.

Harris D., Harris S., Digital Design and Computer Architecture, 2ed, Morgan Kaufmann, 2012.

Pedroni V., Circuit Design and Simulation with VHDL, 2ed, MIT Press, 2010.

Samary Baranov. Logic and System Design of Digital Systems. TTU Press, 2008.

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