VLSI CAD Systems and VLSI Architectures

Credits: 4.00. **Corequisite**: student must take course "Advanced Hardware description language" or "Advanced Digital systems" prior to or concurrently with this course.

No exam in this course, only project (see below).

The course provides design methodology for very complex System-on-Chips (SoC) containing hundreds of millions of gates. This methodology is based on High level or Algorithmic synthesis, converting of the algorithmic behavior into hardware and implementing this behavior. The students will study the modern design tools, performing the full automatic synthesis digital systems from behavioral specification to description in Hardware description languages (VHDL or Verilog) at the Register Transfer Level (RTL). This program will give students the broad and intensive knowledge and skills required to design various digital systems with ASIC and FPGA technologies.

Syllabus: Design of VLSI systems with Hardware Description languages. Design cycle and production process. Design hierarchy. Conceptual, behavioral and structural design. Top-down design methodology. High level Synthesis. Design flow. Construction of Algorithmic State Machines (ASMs) to present the behavior of the designed digital system in GUI or System C or VHDL codes. Time in ASM. Pipeline Processes. Optimized Functional Specification and Project at the Functional Level. Digital system simulation at the High level. Synthesis at the Register Transfer Level (RTL). Digital system as a composition of control unit and date path. External specifications. Generation of VHDL codes for components of Data Path. Generation of VHDL code for Data Path. Design of Control unit in VHDL. Automatic instantiation of Control unit and Data path to construct Top level design in VHDL. Digital system simulation at the Register Transfer Level. Case studies. Design of Controller. Design of Codec. Design of mobile robot. RISC processor design. Each of these designs will be provide in details at the High level and Register Transfer level with simulation and verification at the both levels.

Project in the course. Each two student team will design their version of digital system from external specification till implementation as ASIC (Cadence or Synopsis tools at the RTL level) or FPGA (Xilinx or Altera tools at the RTL level).

Bibliography:

Pedroni V., Circuit Design and Simulation with VHDL, 2ed, MIT Press, 2010.

Baranov S., Logic and System Design of Digital Systems, TTU Press, 2008.

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