Digital Systems Programming Languages (VHDL, VERILOG)
(Syllabus)

Dr. Sinelnikov Vladimir

In this course, the students will study **Hardware Design Language VERILOG** and **VHDL**, which is the important tool, used in the design of electronic circuits and systems. After having studied this course comprising many projects and laboratory works, the student will be ready to use **HDL** for the design of very complicated **VLSI** circuits.

Students should present small project every week. There will be a **"bohan"** within a semester.

Weak 1-3. Hardware description language (VERILOG).
Main language concepts. **MODULE**. Stile of **VLSI** description - Behavioral and Structural stiles. Design Hierarchical levels of design. Design flow. Standard types. Types **nets**, **reg**, and **integer**. User defined integer type. Multi-valued logic types. Arrays in **VERILOG**. Array attributes. **VERILOG** operators. Standard operators. Array operators. Logical operators. Bitwise operators. Comparison operators. Arithmetic operators. Shifting operators. Directives of **VERILOG. Test benches**. Combinational testbench. Verifying responses. Printing response values. The **MODELSYM** using for **VERILOG** simulating

Weeks 4-5. Concurrent and sequential statements. **Initial** and **Always@ blocks** execution. **Sensitivity list**. **Blocked** and **Unblocked** operations. Synthesis of combinational logic. Complete sensitivity list. **If** statement. **Case** statement. Behavior of blocks. **Register transfer level**. Flip-flops. Specifying registers in **VERILOG**.

Weeks 6-7 TASK and **FUNCNUON** in **VERILOG.** Representation of **Finite state machines** (**FSM**) in **VERILOG**. **FSM** initialization. **FSM** flip-flop output signals.

Weeks 8-9. Hardware description language (VHDL).
Main language concepts.
Entity, Architecture, Dataflow, behavioral and structural architectures. Types in **VHDL**. Standard types. Types **bit**, **Boolean, integer**. User Defined integer type. Integer subtypes. Multi-valued logic types. Arrays, Attributes in **VHDL**, Array attributes. **VHDL** operators. Standard operators.
Array operators. Logical operators. Comparison operators. Arithmetic operators.
Shifting operators. Concurrent and sequential statements. Type conversion. Mixing types in expressions Processes, Process execution. Sensitivity list. Synthesis of combinational logic. Complete sensitivity list**. If** statement. **Case** statement. Multiple process calls. Behavior of process. **Wait** statements. **Variable** usage mode. Register transfer level**.** Flip-flops. Specifying registers in **VHDL**.
Detecting a rising clock. Clocked process rules. Package std_logic_arith.
Contents of std_logic_arith. Operators in std_logic_arith. Comparison, Boolean and arithmetic operators.

Weeks 10-11. Representation of **Algorithmic state machines** (**ASM**) and Finite state machines (**FSM**) in **VEILOG** and **VHDL. FSM** initialization. **FSM** flip-flop output

signals. Several modes for **FSM** representation. **Self-checking FSM**, **Berger code checkers**. Verifying responses. **ASM** and **HDL Code coverage**.

Weeks 12. Altera FPGA DE2-115 board project implementation

VERILOG project implementation on **DE2-115** board with the help of **QUARUS II** program

Weeks 13. BOHAN – First attention

Weeks 14/ BOHAN – Second attention

Using Program Instruments:

- **ModelSim,**
- **Quartus II Altera**

Bibliography:

Kaufmann Publishers, 2001.
.-Verilog-2001.com
-Verilog HDL Quick Reference Guide, Verilog-2001 version
Stuart Sutherland
-D. Perry, VHDL (Computer hardware description language), 3d edition,

Percentage grades of course
Libraries: 30%
Bohan: 70%

Students, who missed more than 20% of classes without a good reason (preliminary notification is required) are not allowed to the Bohan. Attendance of the first class is obligatory!

שפות של עיצוב אלגוריתמי ומבני חומרה